Interconnect Systems: Challenges for Nanoelectronics

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Interconnect Systems: Challenges for Nanoelectronics

1. Introduction / Interconnect challenges
2. Diffusion barriers
3. Size effect of interconnect resistivity
4. Porous low k dielectrics
5. Airgap architecture – Key to solve ULK ?
6. Thermal issues
7. Conclusions
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Implementation of new materials in the CMOS process & challenges

Challenges

- risks of new failure modes have to be understood
- customer reliability requirements have to be met

Materials

Source: E. Zschech, AMD Saxony
Modifications: T. Gessner et al., TU Chemnitz
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New metrology in the CMOS manufacturing & challenges

Challenges

- monitor the right parameters
- have the metrology available on time

Source: E. Zschech, AMD Saxony

Modifications: D.R.T. Zahn et al., TU Chemnitz

Year


Materials

Optical microscopy  SEM  TEM  SIMS  AES  TOF-SIMS  FIB  XRR/XRD  Raman  FTIR  ?

AFM-based techniques: SCM, FM/UFM, MicroRaman NanoRaman

LEAP

TEM/STEM/SEM

Cs corr

STM

Scatterometry

Spectroscopic Ellipsometry/Porosimetry

Nanoindentation / SAW

Source: E. Zschech, AMD Saxony

Modifications: D.R.T. Zahn et al., TU Chemnitz
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How to Fight RC Delay: Design, Architecture, Technology

SEM cross-section of AMD Opteron™ and AMD Athlon™64 microprocessors, showing the 9-metal interconnects hierarchy (IEDM 2003, Nanofair 2003)

Low k material as IMD

Hierarchical wiring (reverse scaling)

Photo courtesy: E. Zschech, AMD, Dresden, Germany
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Fabrication of Copper Damascene Interconnects

Trench etched into dielectric

- barrier deposition
- Cu seed layer deposition
- Cu fill
- CMP
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Potential barrier/seed approaches

Available Deposition Processes

- Physical Vapour Deposition (PVD: sputtering, evaporation)
- Chemical Vapour Deposition (CVD)
- Atomic Layer Deposition (ALD)
- Electroless plating

Potential barrier/seed layer approaches

- ALD TaN / PVD Ta / PVD Cu seed
- ALD TaN / CVD Ru seed (direct plating)
- CVD barrier / ALD Cu seed

- WN: example for CVD barrier
  - ALD barriers
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Equipment for TiN/Cu or W(Si)N/Cu CVD

PRECISION 5000™ configuration

- Chamber A: Cu - MOCVD
- Chamber B: WNₓ PECVD
- Chamber C: TiN - MOCVD
- Chamber D: preclean

Process for WNₓ:
PECVD based on \( WF_{6} + N_{2} + H_{2} \)

Available parameters:
- Temperature: 300 - 475°C
- Pressure: 0.1 - 5 Torr
- RF power: 50 - 750 W
- \( WF_{6} \) flow: 100 sccm
- \( N_{2} \) flow: 280 sccm
- \( H_{2} \) flow: 1000 sccm
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10 nm WN Barrier Characterisation / as deposited

- XTEM images of WN$_x$$^3$
  -> Amorphous microstructure
- Electron diffraction pattern of WN$_x$$^3$
  -> Only diffuse rings; reflection spots from a Cu grain

TEM and Electron Diffraction
Comparison of the as deposited state with the state after 400°C/100h

- No significant structural changes
- Barrier remains amorphous
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Atomic Layer Deposition of WCN barrier films

Application of ALD to barrier films

Advantages:
- Highly conformal deposition
- Controlled thickness
- Extremely thin films
- Excellent thickness uniformity

Disadvantages/Challenges:
- Surface sensitivity
- Cost-effective only for very thin films
- For porous and part of low-density low-k materials only applicable at sealed surfaces

Li et al. (ASM, Philips), IITC 2002
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Size effect of interconnect resistivity

W. Hönlein, E. Unger, W. Pamler, Z. Gabric
L. Risch
G. Braun
R. Göttzsche, N. Brüls
H. Wendt
I. Janssen, K. Schober
H. Helneder, U. Seidel
K. Mosig **

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M. Engelhardt et al., Infineon Technologies AG, Corporate Research

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ZFM *
IZM
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S. Schulz
R. Ecke

*cooperation contract with IFX
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Size effect of interconnect resistivity

Nano Interconnects (E-beam litho + IMD etch + TiN/Cu CVD)

E-beam lithography and IMD etch: Infineon CPR NP
Metallization (CVD TiN and Cu): Center for Microtechnologies @ TU Chemnitz

M. Engelhardt et al., Infineon Technologies AG, Corporate Research
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Size effect of interconnect resistivity

Nano Interconnects (Sub-50nm) with high AR (DUV litho & spacer mask)

M. Engelhardt et al., Infineon Technologies AG, Corporate Research
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Size effect of interconnect resistivity

- Barrier thickness reduction
- Interface engineering (reduce interface scattering)
- Cu morphology optimisation (increased grain size, reduced grain boundary scattering)

Resistivity \( [\mu \Omega \text{ cm}] \)

Resistivity \( (\text{Cu}_{\text{bulk}}) = 1.7 \mu \Omega \text{ cm} \)

Measurements:
- Lines \( (L = 200 \mu \text{m}) \)
- Serpentines

Line Width \([\text{nm}]\)


M. Engelhardt et al., Infineon Technologies AG, Corporate Research
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**ITRS Low $k_{eff}$ - Predictions for Cu – Interconnects with low $k$**

*Graph showing the average $K_{eff}$ for Cu-interconnects over time from 1998 to 2018.*
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Ultra low k (materials) concepts

- **dense films**
  - Minimum bulk $k > 1.9$
  - In praxis $> 2.2$

- **porous films**
  - Inherent porosity or introduced by porogens
    - shape of pores,
    - connectivity,
    - pore size distribution
    - (micro $< 2 \text{nm}$, meso $< 50 \text{nm}$)
  - $\Rightarrow$ silica based materials
  - $\Rightarrow$ silsesquioxanes (SSQ)
  - $\Rightarrow$ organic polymers
  - $\diamondsuit$ CVD or spin-on

- **air gaps**
  - Potential of $k_{\text{eff}} < 2.0$
  - Design adaptations needed

How much porosity is needed?
How much porosity can be controlled?

Graphical representation:
- $E \sim \rho^{3.7}$ for porous SiO2
- EMA-model, series and parallel model
- Permittivity vs. porosity in vol% and elastic modulus in GPa

### Interconnect Systems: Challenges for Nanoelectronics

#### Low k dielectric materials: porous films

<table>
<thead>
<tr>
<th>Material</th>
<th>Class</th>
<th>Deposition</th>
<th>$k$</th>
<th>characteristics</th>
<th>Provider</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nanoglass</td>
<td>porous SiO₂</td>
<td>spin on</td>
<td>(2.5...)2.25(... 1.3)</td>
<td>structured porosity (templating)</td>
<td>Allied Signal</td>
</tr>
<tr>
<td>ORION™</td>
<td>C-doped OSG</td>
<td>CVD</td>
<td>2.0-2.2</td>
<td>pore size 1-4nm density 1.04g/cm³</td>
<td>Trikon</td>
</tr>
<tr>
<td>porous SiLK™</td>
<td>aromatized and cross-linked polyphenylene</td>
<td>spin on</td>
<td>2.2-2.0</td>
<td>aver. pore size 6...4nm, pore size distribution range 1..7nm</td>
<td>Dow Chemical</td>
</tr>
<tr>
<td>ZIRKON™</td>
<td>MSQ</td>
<td>spin on</td>
<td>2.2..1.8</td>
<td>small, uniformly distributed pores</td>
<td>Shipley</td>
</tr>
<tr>
<td>LKD 5107</td>
<td>MSQ</td>
<td>spin on</td>
<td>2.2 1.9</td>
<td></td>
<td>JSR Micro</td>
</tr>
<tr>
<td>LKD 6103</td>
<td>MSQ</td>
<td>spin on</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ultra Aurora</td>
<td></td>
<td></td>
<td>2.7..2.5 (2.2)</td>
<td>pore size ~0,5nm</td>
<td>ASM</td>
</tr>
<tr>
<td>CORAL™</td>
<td>SiOC - carbon-doped oxide</td>
<td>Non-PECVD</td>
<td>1.7</td>
<td>structured porosity, very high hardness</td>
<td>Novellus Systems</td>
</tr>
<tr>
<td>FOx™</td>
<td>HSQ</td>
<td>spin on</td>
<td>2.9</td>
<td>microporous</td>
<td>Dow Corning</td>
</tr>
<tr>
<td>BD2</td>
<td>porous SiCOH</td>
<td>CVD</td>
<td>2.5</td>
<td></td>
<td>AMAT</td>
</tr>
</tbody>
</table>

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Materials properties vs. density/porosity

- thermal conductivity vs density
  - \( \lambda = 0.0006 \rho^{0.44} \)
  - \( R^2 = 0.9881 \)

- permittivity vs density
  - trend (power law)
  - LKD JSR, Aerogel TUC

- elastic modulus vs density
  - LKD JSR, Aerogel TUC

the higher the porosity and the lower the density, the lower stiffness and thermal conductivity

increase of thermal and elastic stress during processing and use; serious mechanical issues for CMP and packaging
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Issues of porous low k material in Cu DAMASCENE architecture

- Mechanical stability for metal CMP
- Leakage current sensitive
- Adhesion
- Post via etch clean
- Interface barrier/low k: pore sealing; Impact of etching, stripping on ULK properties;
- Dielectric barrier + cap layer
- Etch stop layer
- Porous film or CVD dielectric (SiO₂ or SiCOH)
- Porous film

Packaging: Mechanically weak dielectric materials (polymers, porous) → supporting patterns
Heat dissipation: Low thermal conductivity dielectric materials → Cu dummy patterns (heat sinks)
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On the Road to lower the k-value of Dielectrics in Cu Interconnects

- Fluor or hydrogen doped SiO$_2$
- Low K: carbon doped SiO$_2$ or organic polymer
- Ultra Low K: Porous SiOC, porous organic polymers

Air gaps (air cavities) = The ultimate solution with conventional interconnects

Dielectric constant

Technological node

- 130 nm
- 90 nm
- 65 nm
- 45 nm
- 32 nm

K = 1

Air gaps

3.8 2.9 2.5 <2.2
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Integration of Porous ULK faces Multiple Challenges

- **Stack deposition:** Plasma treatments for adhesion enhancement
- **Litho:** Resist poisoning, cap layer needed
- **Etch:** Profile (e.g. bowing) and roughness, Low k Modification
- **Strip and clean:** Low k modification
- **Barrier:** Pore sealing, etc.
- **Cu CMP** Adhesion, cracking, collapsing

& architecture for Dual Damascene integration
  e.g. Special hard mask approaches

→ New ULK for every technology node !!

Air gaps requirements: simple, cheap, reliable and scalable
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Airgap Approaches:

- Sacrificial Layer
- Sacrificial Etch
- Decomposition
- Formation by Deposition
  - Nonconformal CVD
  - Selective CVD
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Airgap Approaches:

- Sacrificial Layer
- Sacrificial Etch
- Decomposition

Formation by Deposition:
- Nonconformal CVD
- Selective CVD

Seed layer, nitride, O/TEOS, copper, base layer.
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Airgap Approaches:

- **Formation by Deposition**
  - Nonconformal CVD
  - Selective CVD

<table>
<thead>
<tr>
<th>Sacrificial material</th>
<th>Permanent material</th>
<th>Removal technique</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polymer/resist</td>
<td>p-SiLK/SOG</td>
<td>thermal annealing in N₂</td>
</tr>
<tr>
<td>Unity sacrificial polymer</td>
<td>SiO₂</td>
<td>thermal annealing in N₂</td>
</tr>
<tr>
<td>Carbon</td>
<td>None or SiO₂</td>
<td>thermal annealing in O₂</td>
</tr>
<tr>
<td>SiO₂</td>
<td>SiLK/SiOC/SiC</td>
<td>HF etching</td>
</tr>
</tbody>
</table>
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Airgap Approaches:

- Sacrificial Layer
  - Sacrificial Etch
  - Decomposition
    - Polymer/Resist

Formation by Deposition
- Nonconformal CVD
- Selective CVD

75% of IMD is Air Gap

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Airgap Approaches:

- Sacrificial Layer
  - Sacrificial Etch
    - Removal through defined patterns (patterned mask, spacers, etc.)
  - Decomposition
    - Removal through porous or low density capping layers
  - Removal of SiO$_2$ sacrificial layer by using buffered HF wet etch solution
- Formation by Deposition
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**Air Gap Integration using Buffered HF @ TU Chemnitz – ZfM: Approaches**

### Process Description

Application of a **SACRIFICIAL PECVD SiO\textsubscript{x}** film, finally removed by a **WET ETCH PROCESS** using buffered HF acid

Access control by **HARD MASK** and HF acid **EXPOSURE TIME**

- **Air Gap via MASK**
  - Patterned hard mask defines areas for wet etching attack
  - Wet etching process is aligned by copper lines, a cap- and a sub-layer

- **Air Gap via SPACER**
  - Access to IMD by spacer application
  - Spacer is situated between IMD and copper lines
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Air Gap Integration using Buffered HF @ TU Chemnitz – ZfM: Results

Feasibility for both approaches successfully proven
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Air Gap Integration: Process Integration Challenges

A Local integration is required

– where best electrical performances are necessary
– allows mechanical strength (CMP, Packaging)

Permanent material

Air gaps

Permanent material

Standard Performances Packaging

Cu interconnects

M7-M9

M1-M6

W plugs and active regions
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SEM picture of 10-level dual-Damascene structure fabricated using SILK™ at the lower levels of multilevel interconnects
(T. Ohba, Fujitsu Sci. Tech. J., 38, 1, 2002, Study of current Multilevel Interconnect Technologies for 90 nm and Beyond)

Geometric dimensions of the interconnection system (MPU)

Cross sections of the metallization systems used for simulation (scaled).
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Interconnect Cooling by Heat Sinks

Global lines above unoccupied lower metal levels \( j = 0.5 \text{ MA/cm}^2 \)
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Conclusion

- Nanotechnology in Nanoelectronics is not only due to shrinking dimensions:
  - for interconnects: nanoscale effects like diffusion through ultrathin barriers; dielectrics with 0.5 to 3.0 nm pores – diffusion and conduction/leakage mechanisms; atomic layer deposition gains importance; size effects of conduction in nanoscale interconnects
- Ultrathin barriers available by CVD or ALD – integration is the challenge (especially with CMP & porous ULK dielectrics)
- The favorite ultra low k material is not defined yet – integration issues have been delaying the application for years; $k_{\text{eff}} < 2.5$ ???
- Airgap is a very promising aproach to achieve $k_{\text{eff}} < 2.5$ (even < 2.0) but needs design adaption
- Special design precautions have to be considered to solve thermal issues associated with low thermal conductivity materials (ULK, Airgaps)
- The farer future (> 2015) calls for special nanotechnology interconnect approaches (nanowires, CNT, ... )
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  - Stefan E. Schulz: Copper and low-k integration
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